IN THE SPECIFICATION

Please add the following new paragraph after the paragraph ending on line 1 of page 4:

Figure 5C is a circuit diagram illustrating the details of an alternative embodiment, which operates similar to the embodiment of Figure 5B, but uses a NMOS transistor.

Please amend the paragraph beginning at page 14 line 12 as follows:

Figures 4A, 4B and 4C are circuit diagrams illustrating some of the problems encountered by the use of low voltage transistors in high voltage environment when outp 299 is at 0V. Figures 5A, ~~and~~ 5B, and 5C are circuit diagrams illustrating the manner in which the problems (when outp 299 is at 0V) can be corrected, and additional problems presented even after the corrections when outp 299 is at 3.9V. Figures 5C and 5B differ only in that transistor 410 is implemented in PMOS and NMOS forms respectively. Some advantages of using NMOS form are described in further detail in a section below entitled, "17. Clock Level Selection".